CMOS EXPANDABLE GATES

FEATURES

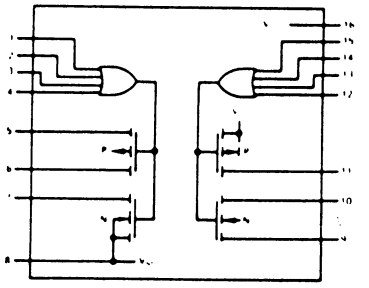
- **Dual 4-Input Gates with Uncommitted Output Transistors**
- **Simplifies Construction of Combinational Logic Functions**
- **CMOS-to-TTL Interface Capability**
- **All Inputs Diode-Protected**

DESCRIPTION

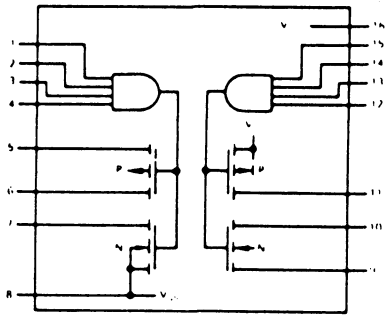
These devices are buffered Dual 4-input NOR Gates (4402B) and NAND Gates (4412B), with uncommitted output transistors. Gate expansion, complex combinational gating, and interface circuits can be constructed from these devices.

LOGIC DIAGRAMS

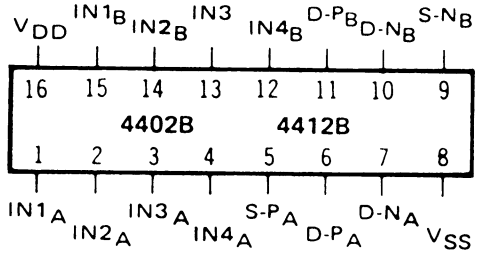
4402B



4412B



CONNECTION DIAGRAM
(all packages)

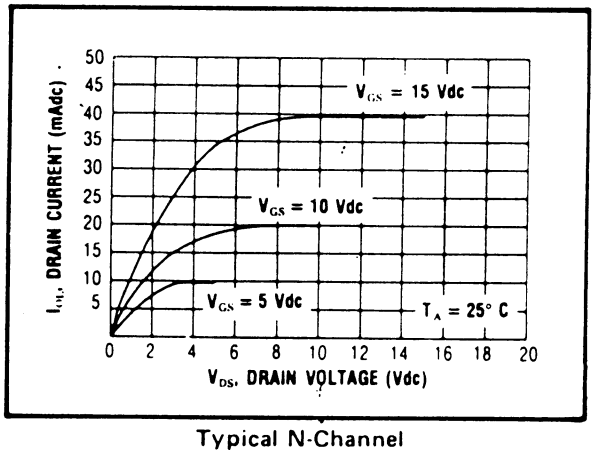


D = Drain
S = Source

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	$V_{DD} - V_{SS}$	3 to 15	Vdc
Operating Temperature	T_A		
C		-55 to +125	°C
E		-40 to +85	°C



Typical N-Channel
Sink Current Characteristics

ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS [1]

PARAMETER		V_{DD} (Vdc)	CONDITIONS	T_{LOW} [2]		+25°C			T_{HIGH} [2]		Units
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	I_{DD}	5	$V_{IN} = V_{SS}$ or V_{DD}	–	0.05	–	0.0005	0.05	–	1.5	μAdc
		10	All valid input	–	0.10	–	0.001	0.10	–	3.0	
		15	combinations	–	0.20	–	0.002	0.20	–	6.0	

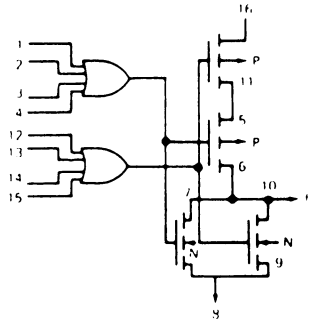
NOTES: [1] Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".
[2] T_{LOW} = -55°C for C
= -40°C for E
T_{HIGH} = +125°C for C
= + 85°C for E

DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V_{DD} (Vdc)	Min.	Typ.	Max.	Units
PROPAGATION DELAY TIME Connected as Dual 4-Input Gates	t_{PLH}, t_{PHL}	5	–	125	250	ns
		10	–	60	120	
		15	–	45	90	
OUTPUT TRANSITION TIME	t_{TLH}, t_{THL}	5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	

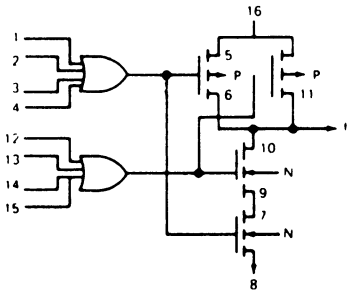
APPLICATIONS INFORMATION

4402B



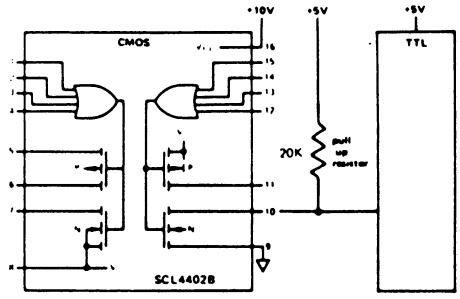
8-Input NOR Configuration

$f = \overline{1 + 2 + 3 + 4 + 12 + 13 + 14 + 15}$



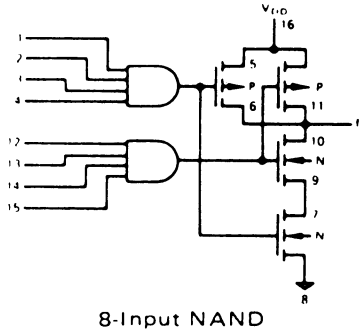
Dual 4-Input OR/NAND Gate

$f = (1 + 2 + 3 + 4) \cdot (12 + 13 + 14 + 15)$



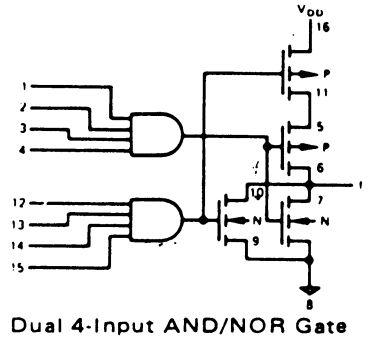
Interfacing CMOS to TTL

4412B



8-Input NAND

$f = \overline{1\,2\,3\,4\,12\,13\,14\,15}$



Dual 4-Input AND/NOR Gate

$f = (1\,2\,3\,4) \cdot (12\,13\,14\,15)$

For additional information, see Application Note AN-102.